

REMARKS

Initially, in the Office Action dated July 17, 2003, the Examiner objects to the specification and the drawings because of informalities. Claims 1-10 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,389,031 (Chao et al.).

By the present response, Applicants have canceled claims 1-10 without disclaimer. Applicants have submitted new claims 11-19 for consideration by the Examiner. Claims 11-19 remain pending in the present application.

Specification Objections

The Examiner has objected to the term NSI on page 7, line 4 of the specification. Applicants have amended the specification to further clarify the invention and respectfully request that this objection be withdrawn.

Drawings Objection

The Examiner has required new corrected drawings for Fig. 5. Applicants have complied with this request and submitted a new amended Fig. 5.

35 U.S.C. §102 Rejections

Claims 1-10 have been rejected under 35 U.S.C. §102(e) as being anticipated by Chao et al. These claims have been canceled therefore rendering these rejections moot.

New Claims

Applicants have submitted new claims 11-19 for consideration by the Examiner. These claims are substantially similar to original claims 1-10. Applicants

respectfully submit that these claims do not contain any prohibited new matter and are patentable over the cited reference.

Chao et al. discloses using a hierarchical searching technique to find the first memory location of a calendar queue with a validity bit of "1" (that is, the lowest time stamp). A number M of bits at level lowest level of the hierarchy correspond to an array of validity bits. M is the largest time stamp. The M bits are grouped into groups $g_{(L-1)}$ bits (where L is the number of levels in the hierarchy). The validity bits in each groups are logically ORed, and then concatenated to define a next level L-2 of bits. That next level of $M/g_{(L-1)}$ bits is further grouped into groups of $g_{(L-2)}$ bits. The process of grouping bits, ORing bits of a group, and concatenating the results is repeated until the resulting string of bits having a predetermined number of bits (e.g., a number of bits that can be placed in a register) is obtained.

Regarding claims 11, 18 and 19, Applicants submit that Chao et al. does not disclose the limitations in the combination of each of these claims of, inter alia, a network forwarding device that includes a router wherein a path information generating unit combines a total of (2^P-1) 2-branch tree nodes comprising one 2-branch tree node and 2-branch tree nodes of $(p-1)$ levels connected to said one 2-branch tree node, into one 2^P -branch tree node and outputs said one 2^P -branch tree node as path information to a path information holding means, wherein said p is an integer equal to or larger than 2, and wherein a next-path searching means checks p bits of a destination address of a packet received at one time and retrieves 2^P -branch tree node corresponding to values of the p bits. Chao et al. relates to an art

of scheduling of packet transmission. In Chao et al., for example, in a switch or router, it is disclosed a layered architecture for retrieving a packet having a minimum time stamp among the packets stored in a plurality of queues which correspond to a plurality of flows. Chao et al. does not disclose or suggest retrieving the information of next path of packet transmission from the destination address, as recited in the claims of the present application. Moreover, Chao et al. does not disclose or suggest path information generating unit combining a total of (2^P-1) 2-branch tree nodes comprising one 2-branch tree node and 2-branch tree nodes of $(p-1)$ levels connected to said one 2-branch tree node, into one 2^P -branch tree node and outputs said one 2^P -branch tree node as said path information to said path information holding means, wherein said p is an integer equal to or larger than 2. The Examiner asserts that this limitation is disclosed in Chao et al. at col. 39, section ii-F, and col. 40, section i-C. Applicants are confused as to which specific portion of Chao et al. the Examiner is referring to since cols. 39 and 49 both disclose the claims of Chao et al., and Applicants cannot find a section ii-F. For the sake of argument, Applicants assume the Examiner refers to claim 10, section i-F and claim 12, section i-C. In any event, the Examiner has misinterpreted Chao et al. as it relates to the limitations in the claims of the present application. These portions of Chao et al. merely disclose that resetting the validity bit includes logically ANDing bit by bit the inverted word and the validity-based bits to generate an AND result, and that updating the validity bits includes logically ORing bit by bit the contents of the storage device of the highest level of the hierarchy I-0 with the first decoded bit word to generate an OR result. In

Chao et al., the validity bits corresponding to the maximum time stamps are divided into a plurality of groups each having a predetermined bits and logical division of the validity bits of each group is taken. By repeating the grouping and taking the logical addition, the groups of validity bits are classified in a layered architecture. This is not a path-information generating unit combining a total of (2^P-1) 2-branch tree nodes that include one 2-branch tree node and 2-branch nodes of $(P-1)$ levels connected to the one 2-branch tree node, into one 2^P -branch tree node, as recited in the claims of the present application. These limitations are not disclosed or suggested in Chao et al.

Regarding claims 12-17, Applicants submit that these claims are dependent on independent claim 11 and, therefore, are patentable at least for the same reasons noted regarding this independent claim.

Accordingly, Applicants submit that Chao et al. does not disclose, suggest or render obvious the limitations in the combination of claims 11-19 of the present application. Applicants respectfully request that these claims be entered and allowed.

In view of the foregoing amendments and remarks, Applicants submit that claims 11-19 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

U.S. Application No. 09/622,484

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (referencing attorney docket no. 500.38900X00).

Respectfully submitted,

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Attachment: Replacement Sheet